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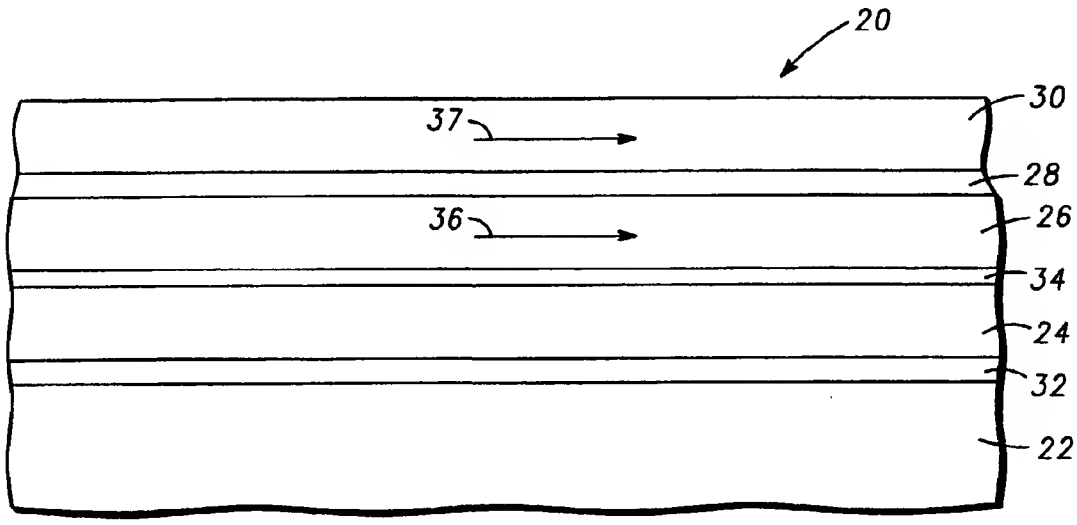

(57) Abstract: A high GMR spin valve structure having multiple layers of a ferromagnetic material (26,30) and a conductive nonmagnetic material (28) can be monolithically integrated with silicon circuits (50) by first growing an accommodating buffer layer (24) on a silicon wafer (22). The accommodating buffer layer is a layer of monocrystalline oxide spaced apart from the silicon wafer by an amorphous oxide layer (32) of silicon oxide. The amorphous oxide layer dissipates strain and permits the growth of a high quality monocrystalline oxide accommodating buffer layer. The accommodating buffer layer is lattice matched to both the underlying silicon wafer and the overlying ferromagnetic layer. Any lattice mismatch between the accommodating buffer layer and the underlying silicon substrate is taken care of by the amorphous oxide layer.

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SPIN VALVE STRUCTURE

Field of the Invention

This invention relates generally to spin valve structures and to a method for their fabrication, and more specifically to an improved spin valve structure and to a method for monolithically integrating the spin valve structure with silicon devices and circuits.

Background of the Invention

Magnetoelectronics (magnetic semiconductor technology) manipulates electrons in semiconductors via electron spin, rather than charge. Spin, like charge, is an inherent physical property of electrons that strongly responds to magnetic fields. Typically, giant magnetoresistive (GMR) material contains a series of layers alternating between a strongly ferromagnetic (capable of being highly magnetized) layer and a magnetically neutral layer. When the magnetic moments in the ferromagnetic layers are aligned, electrons can pass the layered system unimpeded. But applying an external magnetic field can cause successive magnetic layers to have different magnetic alignments, which causes the electrons to be scattered, thus creating a high resistance in the system.

In the past, a variety of magnetic materials and structures have been utilized to form magnetoresistive materials for non-volatile memory elements, read/write heads for disk drives, and other magnetic type applications. Drives storing up to 20 gigabytes are feasible due in part to highly sensitive read heads using magnetic spin valves based on the GMR effect. For example,

the magnetic external field can come from the tiny magnetic domains on the disk, and the strong variation in electrical resistance is used to detect the magnetic orientation on the domains.

It is generally desirable to achieve high GMR ratios in the magnetoelectronic device. High GMR ratios tend to decrease the required sensitivity of the apparatus to sense (read) stored states. One way to increase the GMR is to reduce non-specular electron scattering at the interfaces between the layers. Atomically sharp metal/insulator interfaces are needed to reduce this type of scattering. One such prior apparatus provides a multi-state, magnetic memory cell having a spin polarizing section that includes two magnetic layers positioned in overlying relationship and separated by a non-magnetic layer. The magnetic layers can be ferromagnetically coupled and the non-magnetic layer is a thin layer of electrically conductive material. An example of such a spin polarizing apparatus is disclosed in U.S. Pat. No. 5,838,607 issued to Zhu et al. on Nov. 17, 1998. While this system may provide higher GMR ratios and utilize less sensing and writing current then other prior art systems, the system lacks the ability to monolithically integrate the GMR materials into standard CMOS (or similar integrated circuit) processes.

The vast majority of semiconductor discrete devices and integrated circuits are fabricated from silicon, at least in part because of the availability of inexpensive, high quality monocrystalline silicon substrates. If a spin valve could be realized on a low cost bulk wafer such as a silicon wafer, GMR elements, such as high GMR spin valves, could be monolithically integrated with standard CMOS or similar integrated circuit process. Thereby, providing a commercially viable monolithic structure which takes

advantage of the preferred properties of both the spin valve materials and the silicon.

Accordingly, a need exists for a spin valve structure that provides a high GMR value and a process for monolithically integrating such a structure with standard silicon circuits.

Brief Description of the Drawings

The present invention is illustrated by way of example and not limitation in the accompanying figures, in which like references indicate similar elements, and in which:

FIGS. 1, 6 and 8-12 illustrate schematically, in cross section, device structures in accordance with various embodiments of the invention;

FIGS. 2-5 illustrate several possible relative positions of magnetic vectors in accordance with various embodiments of the invention; and

FIG. 7 illustrates graphically the relationship between maximum attainable film thickness and lattice mismatch between a host crystal and a grown crystalline overlayer.

Skilled artisans will appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help to improve understanding of embodiments of the present invention.

Detailed Description of the Drawings

FIG. 1 illustrates schematically, in cross section, a portion of a spin valve structure 20 in accordance with an embodiment of the invention. Spin valve structure 20 includes a monocrystalline substrate 22, an accommodating buffer layer 24 comprising a monocrystalline material, a ferromagnetic layer 26, a conductive non-magnetic layer 28, and a ferromagnetic layer 30. In this context, the terms "monocrystalline" and "ferromagnetic" shall have the meaning commonly used within the semiconductor industry. "Monocrystalline" shall refer to materials that are a single crystal or that are substantially a single crystal and shall include those materials having a relatively small number of defects such as dislocations and the like as are commonly found in substrates of silicon or germanium or mixtures of silicon and germanium and epitaxial layers of such materials commonly found in the semiconductor industry. "Ferromagnetic" shall refer to materials that contain atomic magnetic moments that tend to align parallel to each other even in a weak external magnetic field and may remain magnetized even after the external field is removed.

In accordance with one embodiment of the invention, structure 20 also includes an amorphous oxide layer 32 positioned between substrate 22 and accommodating buffer layer 24. Structure 20 may also include a template layer 34 between the accommodating buffer layer and ferromagnetic layer 26. As will be explained more fully below, the template layer helps to initiate the growth of the ferromagnetic layer on the accommodating buffer layer. The amorphous oxide layer helps to relieve the strain in the accommodating buffer layer and by doing so, aids in the growth of a high crystalline quality accommodating buffer layer.

Substrate 22, in accordance with an embodiment of the invention, is a monocrystalline semiconductor wafer, preferably of large diameter. The wafer can be of a material from Group IV of the periodic table, and preferably a material from Group IVA. Examples of Group IV semiconductor materials include silicon, germanium, mixed silicon and germanium, mixed silicon and carbon, mixed silicon, germanium and carbon, and the like. Preferably substrate 22 is a wafer containing silicon or germanium, and most preferably is a high quality monocrystalline silicon wafer as used in the semiconductor industry.

Accommodating buffer layer 24 is preferably a monocrystalline oxide or nitride material epitaxially grown on the underlying substrate. In accordance with one embodiment of the invention, amorphous oxide layer 32 is grown on substrate 22 at the interface between substrate 22 and the growing accommodating buffer layer 24 by the oxidation of substrate 22 during the growth of layer 24. The amorphous oxide layer serves to relieve strain that might otherwise occur in the monocrystalline accommodating buffer layer as a result of differences in the lattice constants of the substrate and the buffer layer. As used herein, lattice constant refers to the distance between atoms of a cell measured in the plane of the surface. If such strain is not relieved by the amorphous oxide layer, the strain may cause defects in the crystalline structure of the accommodating buffer layer. Defects in the crystalline structure of the accommodating buffer layer, in turn, would make it difficult to achieve a high quality crystalline structure in preferably monocrystalline ferromagnetic layers 26 and 30 and preferably monocrystalline conductive non-magnetic layer 28.

Accommodating buffer layer 24 is preferably selected for its crystalline compatibility with the underlying

substrate and with the overlying ferromagnetic material. For example, the material could be an oxide or nitride having a lattice structure matched to the substrate and to the subsequently applied ferromagnetic material.

Materials that are suitable for the accommodating buffer layer include metal oxides such as the alkaline earth metal titanates, alkaline earth metal zirconates, alkaline earth metal hafnates, alkaline earth metal tantalates, alkaline earth metal ruthenates, alkaline earth metal niobates, alkaline earth metal vanadates, perovskite oxides such as alkaline earth metal tin-based perovskites, lanthanum aluminate, lanthanum scandium oxide, and gadolinium oxide. Additionally, various metal nitrides such as gallium nitride and aluminum nitride may also be used for the accommodating buffer layer. Most of these materials are insulators, although strontium ruthenate, for example, is a conductor. Generally, these materials are metal oxides or metal nitrides, and more particularly, these metal oxide or nitrides typically include at least two different metallic elements. In some specific applications, the metal oxides or nitride may include three or more different metallic elements.

Amorphous oxide layer 32 is preferably an oxide formed by the oxidation of the surface of substrate 22, and more preferably is composed of a silicon oxide. The thickness of layer 32 is sufficient to relieve strain attributed to mismatches between the lattice constants of substrate 22 and accommodating buffer layer 24. Typically layer 32 has a thickness in the range of approximately 0.5-5 nm.

The ferromagnetic material of layers 26 and 30 can be selected as needed for a particular spin valve structure and can generally be characterized as $(A_xB_{1-x})CO_3$, where A may be lanthanum or neodymuium, and $0 \geq x \leq 1$; B may be strontium, barium, calcium or lead, C may be manganese or

a manganese compound such as manganese cobalt (Mn_yCo_{1-y}) where $0 > y \leq 1$, and manganese nickel (Mn_zNi_{1-z}) where $0 > z \leq 1$. In addition, layers 26 and 30 are preferably monocrystalline. Typically layers 26 and 30 have a thickness in the range of approximately 1-200 nm and preferably in the range of about 2-50 nm.

Electrically conductive non-magnetic layer 28 is sandwiched between ferromagnetic layer 26 and ferromagnetic layer 30. Layer 28 can suitably include any conducting non-magnetic material and is preferably an electrically conductive monocrystalline oxide. Examples of suitable materials for layer 28 include $(La_kSr_{1-k})CoO_3$ (lanthanum strontium cobalt oxide) where $0 > k < 1$, and $SrVO_3$ (strontium vanadium oxide). Typically layer 28 is thinner than ferromagnetic layers 26 and 30 and has a thickness in the range of approximately 0.5-20 nm and preferably in the range of about 1-10 nm.

Suitable template materials chemically bond to the surface of the accommodating buffer layer 24 at selected sites and provide sites for the nucleation of the epitaxial growth of subsequent ferromagnetic layer 26. Template layer 34 is formed by capping the oxide layer 24 and preferably has a thickness of 1-10 monolayers. Appropriate materials for template layer 34 may be chosen as needed for a particular application. For example, in the present embodiment, suitable materials for template layer 34 include oxygen and strontium, barium, calcium, or lead.

Spin valves react strongly in the presence of an applied magnetic field. The external magnetic field changes the magnetic alignment of the ferromagnetic layers which causes the entering electrons to scatter, thus creating high resistance in the system. The magnetization of one or both of layers 26 and 30 may be changed under an applied magnetic field and, for exemplary purposes,

magnetic vectors 36 and 37 for layers 26 and 30 respectively, are illustrated as being both directed in the same direction. When the magnetic moments of the two ferromagnetic layers 26 and 30 are aligned, the resistance for an entering electron is relatively small. Thus the electrons can pass through the layered system generally unimpeded.

Referring now to FIGS. 2-5, four different states or position combinations of magnetic vectors 36 and 37 are illustrated schematically for spin valve structure 20. The examples illustrated in FIGS. 2-5 are ordered in accordance with the resistance of the structure, from the lowest resistance in FIG. 2 to the highest resistance in FIG. 5. The orientation of vectors 36 and 37 is the same in FIG. 2 as in FIG.1, where both vectors are directed in the same direction. Thus, the electrons will travel a relatively straight path through structure 20 and the resistance will be minimum. In FIG. 3, both magnetic vectors 36 and 37 are directed in the same direction but opposite of the vector directions in FIG. 2. Thus, the resistance for the entering electrons is relatively small and the electrons will pass through structure 20 generally unimpeded. However, in FIGS. 4 and 5, magnetic vectors 36 and 37 are directed opposite each other, thus causing the entering electrons to be scattered creating a high resistance.

Non-specular electron scattering at the interfaces of the layers in the spin valve tends to limit the magnetoresistive values. Ideal surfaces and layer interfaces would provide specular scattering and help to increase the electron near free path which in turn helps to increase the GMR. One way to improve the GMR is to provide epitaxial, atomically sharp, metal/insulator interfaces in the spin valve structure. To accomplish this, any known deposition process where the monolayer

deposition is controlled is suitable. Examples of such deposition processes include molecular beam epitaxy (MBE), atomic layer epitaxy (ALE), and some chemical vapor deposition (CVD) processes, all of which are well known in the semiconductor industry.

In accordance with one embodiment of the invention, a spin valve structure is grown in an oxide system where a monocrystalline insulator such as strontium titanate oxide (STO), one or more monocrystalline ferromagnetic layers such as LSMO (lanthanum strontium manganese oxide), and a monocrystalline conductive, non-magnetic metal such as LSCO (lanthanum strontium cobalt oxide)are all grown epitaxially with atomically flat interfaces. In addition, the spin valve structure of the present embodiment can be grown epitaxially on a monocrystalline silicon substrate using a monocrystalline amorphous buffer layer such as SiO_2 (silicon oxide) to enable GMR elements to be monolithically integrated with silicon circuits.

FIG. 6 illustrates schematically, in cross section, a portion of a spin valve structure 40 in accordance with another embodiment of the invention. Structure 40 is similar to spin valve structure 20 except an additional layer 42 of electrically conductive non-magnetic material and an additional layer 44 of ferromagnetic material are added. Layer 42 suitably includes any of the previously disclosed materials for conductive non-magnetic oxide layer 28 and is grown atop ferromagnetic layer 30. Additional layer 44 suitably includes any of the previously disclosed materials for ferromagnetic layers 26 and 30 and is grown atop additional layer 42 of conductive non-magnetic oxide. Typically, as the number of layers increases, a stronger magnetic field is required to switch the magnetic moments of the ferromagnetic layers. However, as the number of layers increases, the magnetoresistive effect of the system generally increases.

Therefore, the layering could continue until ideally a GMR > 100% is achieved.

In accordance with another exemplary embodiment of the invention, the monocrystalline accommodating buffer layer and the oxide layer are exposed to an anneal process such that the buffer and oxide layers form an amorphous oxide layer (not shown).

In accordance with one embodiment of the invention, monocrystalline substrate 22 is a silicon substrate oriented in the (100) direction. The silicon substrate can be, for example, a silicon substrate as is commonly used in making complementary metal oxide semiconductor (CMOS) integrated circuits having a diameter of about 200-300 mm. In accordance with this embodiment of the invention, accommodating buffer layer 24 is a monocrystalline layer of $Sr_zBa_{1-z}TiO_3$ where z ranges from 0 to 1 and the amorphous oxide layer is a layer of silicon oxide (SiO_x) formed at the interface between the silicon substrate and the accommodating buffer layer. The value of z is selected to obtain one or more lattice constants closely matched to corresponding lattice constants of the subsequently formed layer 26. The accommodating buffer layer can have a thickness of about 2 to about 100 nanometers (nm) and preferably has a thickness of about 10 nm. In general, it is desired to have an accommodating buffer layer thick enough to isolate the ferromagnetic layer from the substrate to obtain the desired electrical and magnetic properties. Layers thicker than 100 nm usually provide little additional benefit while increasing cost unnecessarily; however, thicker layers may be fabricated if needed. The amorphous oxide layer of silicon oxide can have a thickness of about 0.5-5 nm, and preferably a thickness of about 1.5-2.5 nm.

To facilitate the epitaxial growth of the ferromagnetic material on the monocrystalline oxide, by

way of a preferred example, 1-10 monolayers of Ti-O, Sr-O, or Ba-O have been shown to successfully grow the ferromagnetic layer.

In accordance with a further embodiment of the invention, monocrystalline substrate 22 is a silicon substrate as described above. The accommodating buffer layer is a monocrystalline oxide of strontium or barium zirconate or hafnate in a cubic or orthorhombic phase with an amorphous oxide layer of silicon oxide formed at the interface between the silicon substrate and the accommodating buffer layer. The accommodating buffer layer can have a thickness of about 2-100 nm and preferably has a thickness of at least 5 nm to ensure adequate crystalline and surface quality and is formed of a monocrystalline $SrZrO_3$, $BaZrO_3$, $SrHfO_3$, $BaSnO_3$ or $BaHfO_3$. For example, a monocrystalline oxide layer of $BaZrO_3$ can grow at a temperature of about 700 degrees C. The lattice structure of the resulting crystalline oxide exhibits a 45 degree rotation with respect to the substrate silicon lattice structure.

Substrate 22 is a monocrystalline substrate such as a monocrystalline silicon substrate. The crystalline structure of the monocrystalline substrate is characterized by a lattice constant and by a lattice orientation. In similar manner, accommodating buffer layer 24 is also a monocrystalline material and the lattice of that monocrystalline material is characterized by a lattice constant and a crystal orientation. The lattice constants of the accommodating buffer layer and the monocrystalline substrate must be closely matched or, alternatively, must be such that upon rotation of one crystal orientation with respect to the other crystal orientation, a substantial match in lattice constants is achieved. In this context the terms "substantially equal" and "substantially matched" mean that there is sufficient

similarity between the lattice constants to permit the growth of a high quality crystalline layer on the underlying layer.

FIG. 7 illustrates graphically the relationship of the achievable thickness of a grown crystal layer of high crystalline quality as a function of the mismatch between the lattice constants of the host crystal and the grown crystal. Curve 46 illustrates the boundary of high crystalline quality material. The area to the right of curve 46 represents layers that tend to be polycrystalline. With no lattice mismatch, it is theoretically possible to grow an infinitely thick, high quality epitaxial layer on the host crystal. As the mismatch in lattice constants increases, the thickness of achievable, high quality crystalline layer decreases rapidly. As a reference point, for example, if the lattice constants between the host crystal and the grown layer are mismatched by more than about 2%, monocrystalline epitaxial layers in excess of about 20 nm cannot be achieved.

In accordance with one embodiment of the invention, substrate 22 is a (100) or (111) oriented monocrystalline silicon wafer and accommodating buffer layer 24 is a layer of strontium barium titanate. Substantial matching of lattice constants between these two materials is achieved by rotating the crystal orientation of the titanate material by 45° with respect to the crystal orientation of the silicon substrate wafer. The inclusion in the structure of amorphous oxide layer 32, a silicon oxide layer in this example, if it is of sufficient thickness, serves to reduce strain in the titanate monocrystalline layer that might result from any mismatch in the lattice constants of the host silicon wafer and the grown titanate layer. As a result, in accordance with an embodiment of

the invention, a high quality, thick, monocrystalline titanate layer is achievable.

Layer 26 (and subsequent layer 30) is a layer of epitaxially grown monocrystalline material and that crystalline material is also characterized by a crystal lattice constant and a crystal orientation. In accordance with one embodiment of the invention, the lattice constant of layer 26 differs from the lattice constant of substrate 22. To achieve high crystalline quality in this epitaxially grown monocrystalline layer, the accommodating buffer layer must be of high crystalline quality. In addition, in order to achieve high crystalline quality in layer 26, substantial matching between the crystal lattice constant of the host crystal, in this case, the monocrystalline accommodating buffer layer, and the grown crystal is desired. With properly selected materials this substantial matching of lattice constants is achieved as a result of rotation of the crystal orientation of the grown crystal with respect to the orientation of the host crystal. In some instances, a crystalline buffer layer between the host oxide and the grown ferromagnetic layer can be used to reduce strain in the grown monocrystalline ferromagnetic layer that might result from small differences in lattice constants. Better crystalline quality in the grown monocrystalline ferromagnetic layer can thereby be achieved.

Layer 28 is a layer of epitaxially grown monocrystalline material and that crystalline material is also characterized by a crystal lattice constant and a crystal orientation. In accordance with one embodiment of the invention, layer 28 is substantially lattice matched to layer 26.

FIG. 8 illustrates schematically, in cross section, a portion of a spin valve structure 50 in accordance with another embodiment of the invention. Structure 50 is

similar to the previously described spin valve structure 20, except that an additional template layer 48 is positioned between amorphous oxide layer 32 and monocrystalline substrate 22. The additional template layer 48, formed of an alkali earth metal or alkali earth oxide, serves to provide a growth facilitating surface for the nucleation of the epitaxial growth of monocrystalline accommodating buffer layer 24. An alkali earth metal or oxide including Ba, Sr, Ba-Sr, Ba-O, Sr-O and Ba-Sr-O is deposited onto monocrystalline substrate 22 of preferably silicon and having a silicon oxide layer (not shown) on its surface. The substrate is heated to a temperature sufficient to cause the alkali earth metal or oxide to react with the native silicon oxide layer. The resulting surface forms additional template layer 48.

FIG. 9 illustrates schematically, in cross section, a spin valve structure 60 in accordance with a further embodiment of the invention. Structure 60 includes a monocrystalline semiconductor substrate 52, preferably a monocrystalline silicon wafer. Monocrystalline semiconductor substrate 52 includes two regions, 53 and 54. An electrical semiconductor component generally indicated by the dashed line 56 is formed in region 53. Electrical component 56 can be a resistor, a capacitor, an active semiconductor component such as a diode or a transistor or an integrated logic element or circuit such as a CMOS integrated circuit and formed by conventional semiconductor processing as is well known and widely practiced in the industry. A layer of insulating material 58 such as a layer of silicon dioxide or the like may overlie electrical semiconductor component 56 to, for example, protect the underlying component from the environment and avoid short circuiting within the structure.

Insulating material 58 and any other layers that may have been formed or deposited during the processing of semiconductor component 56 in region 53 are removed from the surface of region 54 to provide a bare silicon surface in that region. As is well known, bare silicon surfaces are highly reactive and a native silicon oxide layer can quickly form on the bare surface. In one embodiment, a layer of barium or barium and oxygen is deposited onto the native oxide layer on the surface of region 54 and is reacted with the oxidized surface to form a template layer (not shown). A monocrystalline oxide layer 62 is formed overlying the template layer. An amorphous oxide layer 61 is formed underlying monocrystalline oxide layer 62. In yet another embodiment, another template layer (not shown) is formed overlying monocrystalline oxide layer 62.

A ferromagnetic layer 64 is epitaxially grown overlying monocrystalline oxide layer 62 or alternatively a template layer (not shown). An electrically conductive non-magnetic oxide layer 66 is epitaxially grown atop ferromagnetic layer 64. An additional ferromagnetic layer 68 is epitaxially grown overlying layer 66.

In accordance with a further embodiment of the invention, ferromagnetic layers 64 and 68 and oxide layer 66 are photolithographically patterned to form a magnetic sensor, generally indicated by a dashed line 69. In one embodiment, sensor 69 can suitably detect the presence of a magnetic field on the magnetic layers of spin valve 60 and, preferably, magnetic sensor 69 includes a memory element which can suitably detect the dipole state of the magnetic layer by sensing the magnetic material. In accordance with one aspect of the present embodiment, a layer of conductive material (not shown) can be deposited atop magnetic sensor 69 and component 56 which is preferably a CMOS circuit. The layer of conductive material (such as a metal) aids to electrically connect

sensor 69 and component 56. In accordance with one aspect of the present embodiment and known photolithographic processes, a layer of photoresist is deposited where the pattern is desired. The pattern is transferred by known processes and unexposed photoresist is removed. A metallic conductor, schematically indicated by a line 70, is etched back to electrically couple component 56 and sensor 69.

FIG. 10 illustrates schematically, in cross section, a spin valve structure 80 in accordance with another embodiment of the invention. Structure 80 is similar to spin valve structure 60 except that a metallic conductor, schematically indicated by a line 82, electrically couples component 56 and electrically conductive non-magnetic oxide layer 66. Preferably layer 66 is monocrystalline and component 56 is for example an integrated logic circuit such as a CMOS circuit. The present embodiment may be formed, for example, in a similar photolithographic process as described for structure 60 where patterning layers 64, 66 and 68 expose a portion of component 56 and then an electrical interconnection from component 56 to layer 66 is formed.

FIG. 11 illustrates schematically, in cross section, a spin valve structure 85 in accordance with yet another embodiment of the invention. Structure 85 is similar to spin valve structure 80 except that an additional electrically conductive non-magnetic oxide layer 84 and an additional ferromagnetic layer 86 are added. In a similar manner as previously discussed for spin valve structure 40, layers 84 and 86 are epitaxially grown atop ferromagnetic layer 68. In accordance with one aspect of the present embodiment, a metallic conductor, schematically indicated by a line 88, can be formed to electrically couple layer 66 of preferably monocrystalline electrically conductive non-magnetic oxide and layer 84 of

preferably monocrystalline electrically conductive non-magnetic oxide. Structure 85 can be patterned in a similar manner as previously discussed for structures 60 and 80.

The following example illustrates a process, in accordance with one embodiment of the invention, for fabricating a spin valve structure such as the structures depicted in FIGS. 1-11 and more specifically FIG. 12 and a spin valve structure 90. The process starts by providing a monocrystalline semiconductor substrate 92 of silicon or germanium. In accordance with a preferred embodiment of the invention, the semiconductor substrate is a silicon wafer having a (100) orientation. The substrate is preferably oriented on axis or, at most, about 0.5° off axis. At least a portion of the semiconductor substrate has a bare surface, although other portions of the substrate, as described below, may encompass other structures. The term "bare" in this context means that the surface in the portion of the substrate has been cleaned to remove any oxides, contaminants, or other foreign material. As is well known, bare silicon is highly reactive and readily forms a native oxide. The term "bare" is intended to encompass such a native oxide. A thin silicon oxide (not shown) may also be intentionally grown on the semiconductor substrate, although such a grown oxide is not essential to the process in accordance with the invention.

In order to epitaxially grow a monocrystalline oxide layer 94 overlying monocrystalline substrate 92, the native oxide layer must first be removed to expose the crystalline structure of the underlying substrate. The following process is preferably carried out by molecular beam epitaxy (MBE), although other epitaxial processes may also be used in accordance with the present invention. The native oxide can be removed by first thermally

depositing a thin layer alkali earth metal or alkali earth metal oxide such as strontium, barium, a combination of strontium and barium, strontium oxide or barium strontium oxide in an MBE apparatus. The substrate is then heated to a temperature in the range of approximately 200° C to 800° C. In the case where strontium is used, the substrate is then heated to a temperature of about 750° C to cause the strontium to react with the native silicon oxide layer. The strontium serves to reduce the silicon oxide to leave a silicon oxide-free surface. The resultant surface, which exhibits an ordered 2x1 structure, includes strontium, oxygen, and silicon. The ordered 2x1 structure forms a template (not shown) for the ordered growth of an overlying layer 94 of monocrystalline oxide. The template provides the necessary chemical and physical properties to nucleate the crystalline growth of an overlying layer.

In accordance with an alternate embodiment of the invention, the native silicon oxide can be converted and the substrate surface can be prepared for the growth of monocrystalline oxide layer 94 by depositing an alkali earth metal oxide, such as strontium oxide, strontium barium oxide, or barium oxide, onto the substrate surface by MBE at a low temperature and by subsequently heating the structure to a temperature of about 750°C. At this temperature a solid state reaction takes place between the strontium oxide and the native silicon oxide causing the reduction of the native silicon oxide and leaving an ordered 2x1 structure with strontium, oxygen, and silicon remaining on the substrate surface. Again, this forms a template (not shown) for the subsequent growth of ordered monocrystalline oxide layer 94.

Following the removal of the silicon oxide from the surface of the substrate, in accordance with one embodiment of the invention, the substrate is cooled to a

temperature in the range of about 200-800°C and a layer of titanium, oxygen and strontium, barium or a combination of strontium and barium is grown on the template layer by molecular beam epitaxy. The MBE process is initiated by opening shutters in the MBE apparatus to expose strontium, titanium and oxygen sources. The ratio of strontium and titanium is approximately 1:1. The partial pressure of oxygen is initially set at a minimum value to grow , for example, stochiometric strontium titanate at a growth rate of about 0.3-0.5 nm per minute. After initiating growth of the strontium titanate, the partial pressure of oxygen is increased above the initial minimum value. The overpressure of oxygen causes the growth of an amorphous silicon oxide layer 93 at the interface between the underlying substrate and the growing strontium titanate layer 94. The growth of the silicon oxide layer 93 results from the diffusion of oxygen through the growing strontium titanate layer to the interface where the oxygen reacts with silicon at the surface of the underlying substrate. The strontium titanate grows as an ordered monocrystal with the crystalline orientation rotated by 45° with respect to the ordered 2x1 crystalline structure of the underlying substrate. Strain that otherwise might exist in the strontium titanate layer 94 because of the small mismatch in lattice constant between silicon substrate 92 and the growing crystal is relieved in amorphous silicon oxide layer 93.

After strontium titanate layer 94 has been grown to the desired thickness, the monocrystalline strontium titanate is capped by a template layer (not shown) that is conducive to the subsequent growth of an epitaxial monocrystalline layer 96 of a desired ferromagnetic material. In accordance with one embodiment of the invention, lanthanum strontium manganese oxide (LSMO) is deposited on strontium titanate layer 94 by MBE in a

similar manner as previously discussed. LSMO layer 96 grows as an ordered crystalline structure, due largely in part, to the highly crystalline layers underlying layer 96.

As is typical for spin valve structures in the industry, a layer of conducting non-magnetic material is sandwiched between two ferromagnetic layers. A layer 98 of electrically conductive non-magnetic material is epitaxially grown atop LSMO layer 96, followed by another LSMO layer 100. In accordance with one aspect of the present embodiment, layer 98 is lanthanum strontium cobalt oxide (LSCO).

In accordance with another embodiment of the invention, the multiple layers of structure 90 are deposited by a controlled monolayer process such as MBE. The interfaces between layers 100 and 98, layers 98 and 96, and layers 96 and 94 are thus atomically sharp which helps to reduce non-specular scattering at the interfaces and increase the GMR value.

Ferromagnetic layers typically exhibit some conductivity which can interfere with the desired operation of the spin valve structure. For example, in the presence of a magnetic field (passing a current through the structure), the magnetic dipoles of the two ferromagnetic LSMO layers 96 and 100 are altered and resistance of the system increases. It is often desirable to insulate the top ferromagnetic layer by depositing a layer of insulating material on the uppermost surface of the structure. In accordance with the present embodiment, a layer of silicon dioxide 102 is deposited atop LSMO layer 100 to, among other things, offer an insulating layer between the ferromagnetic material of LSMO layer 100 and subsequent metal layer 104. Metal layer 104 is deposited atop silicon dioxide layer 102 to induce the magnetic field.

In another aspect of the present embodiment, a metal layer 106 is deposited atop LSCO layer 98 to create a contact point with layer 98. In one exemplary embodiment, layer 106 is a sense or read path and layer 104 is a word or write line.

The process described above illustrates a process for forming a spin valve structure including a silicon substrate, an overlying oxide layer, one or more ferromagnetic layers, and a conducting oxide layer by the process of molecular beam epitaxy. The process can also be carried out by the process of chemical vapor deposition (CVD), metal organic chemical vapor deposition (MOCVD), migration enhanced epitaxy (MEE), atomic layer epitaxy (ALE), physical vapor deposition (PVD), chemical solution deposition (CSD), pulsed laser deposition (PLD), or the like. Further, by a similar process, other monocrystalline accommodating buffer layers such as alkaline earth metal titanates, zirconates, hafnates, tantalates, vanadates, ruthenates, and niobates, peroskite oxides such as alkaline earth metal tin-based perovskites, lanthanum aluminate, lanthanum scandium oxide, and gadolinium oxide can also be grown. Further, by a similar process such as MBE, other monocrystalline ferromagnetic layers and conductive non-magnetic layers can be deposited overlying the monocrystalline oxide accommodating buffer layer.

Each of the variations of ferromagnetic materials and monocrystalline oxide accommodating buffer layer uses an appropriate template for initiating the growth of the ferromagnetic layer. For example, if the accommodating buffer layer is an alkaline earth metal zirconate, the oxide can be capped by a thin layer of zirconium. Similarly, if the monocrystalline oxide accommodating buffer layer is an alkaline earth metal hafnate, the oxide layer can be capped by a thin layer of hafnium. In a

similar manner, strontium titanate can be capped with a layer of strontium or strontium and oxygen and barium titanate can be capped with a layer of barium or barium and oxygen.

In the foregoing specification, the invention has been described with reference to specific embodiments. However, one of ordinary skill in the art appreciates that various modifications and changes can be made without departing from the scope of the present invention as set forth in the claims below. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of present invention.

Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential features or elements of any or all the claims. As used herein, the terms "comprises," "comprising," or any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a list of elements does not include only those elements but may include other elements not expressly listed or inherent to such process, method, article, or apparatus.

CLAIMS

1. A spin valve structure comprising:

a monocrystalline semiconductor substrate;

a monocrystalline insulator layer overlying the substrate;

a first layer epitaxially grown overlying the monocrystalline insulator layer, the first layer capable of exhibiting ferromagnetic properties;

a second electrically conductive non-magnetic layer epitaxially grown overlying the first layer; and

a third layer overlying the second electrically conductive non-magnetic layer, the third layer capable of exhibiting ferromagnetic properties.

2. The structure of claim 1 wherein the first layer and the second layer are each monocrystalline.

3. The structure of claim 2 wherein the third layer is monocrystalline.

4. The structure of claim 1 wherein the substrate comprises silicon.

5. The structure of claim 4 further comprising a CMOS circuit formed at least partially in the substrate.

6. The structure of claim 1 wherein the monocrystalline insulating layer comprises a material selected from the group consisting of metal oxides and metal nitrides.

7. The structure of claim 6 wherein the monocrystalline insulating layer comprises a material selected from the group consisting of alkali earth metal titanates, zirconates, hafnates, tantalates, ruthenates, niobates and vanadates, perovskites including tin based perovskites, lanthanum aluminate, lanthanum scandium oxide, gadolinium oxide, gallium nitride, and aluminum nitride.

8. The structure of claim 6 wherein the first layer comprises a manganite perovskite.

9. The structure of claim 6 wherein the first layer comprises a material having a composition $(A_xB_{1-x})CO_3$ where A is selected from the group consisting of lanthanum and neodymium, B is selected from the group consisting of strontium, barium, calcium, and lead and x ranges from 0 to 1, and C is selected from the group consisting of Mn, (Mn_yCo_{1-y}) where y is greater than zero and less than or equal to 1, and (Mn_zNi_{1-z}) where z is greater than 0 and equal to or less than 1.

10. The structure of claim 9 wherein the first layer comprises a monocrystalline oxide.

11. The structure of claim 9 further comprising a template layer overlying the monocrystalline insulator layer.

12. The structure of claim 11 wherein the template layer terminates the monocrystalline insulator layer and comprises a layer comprising oxygen and an element selected from the group consisting of strontium, barium, calcium, and lead.

13. The structure of claim 12 wherein the template layer has a thickness of 1 - 10 monolayers.

14. The structure of claim 6 wherein the third layer comprises a manganite perovskite.

15. The structure of claim 6 wherein the third layer comprises a material having a composition $(A_xB_{1-x})CO_3$ where A is selected from the group consisting of lanthanum and neodymium, B is selected from the group consisting of strontium, barium, calcium, and lead and x ranges from 0 to 1, and C is selected from the group consisting of Mn, (Mn_yCo_{1-y}) where y is greater than zero and less than or equal to 1, and (Mn_zNi_{1-z}) where z is greater than 0 and equal to or less than 1.

16. The structure of claim 15 wherein the third layer comprises a monocrystalline oxide.

17. The structure of claim 6 wherein the second electrically conductive non-magnetic layer comprises an electrically conductive oxide.

18. The structure of claim 17 wherein the second electrically conductive non-magnetic layer comprises a material selected from the group consisting of $(La_kSr_{1-k})CoO_3$ where k is greater than 0 and less than 1 and $SrVO_3$.

19. The structure of claim 17 wherein the second electrically conductive layer comprises a monocrystalline oxide.

20. The structure of claim 1 wherein the second electrically conductive layer has a thickness of about 1 - 10nm and the first layer and the third layer each have a thickness of about 2 - 50nm.

21. The structure of claim 1 further comprising an amorphous oxide layer formed underlying the monocrystalline insulator layer.

22. The structure of claim 1 further comprising an integrated logic element formed at least partially in the substrate.

23. The structure of claim 22 wherein the first layer, second electrically conductive non-magnetic layer, and the third layer are patterned to form, in part, a magnetic sensor.

24. The structure of claim 23 wherein the magnetic sensor comprises a memory element.

25. The structure of claim 24 further comprising an interconnection formed between and electrically interconnecting the integrated logic element and the memory element.

26. The structure of claim 1 wherein each of the first layer, second electrically conductive non-magnetic layer, and the third layer comprises a layer of material having an ordered crystalline structure.

27. A spin valve structure comprising:

a monocrystalline semiconductor substrate;

a monocrystalline oxide layer epitaxially grown overlying the substrate;

a first layer of ferromagnetic material overlying the monocrystalline oxide layer and forming an atomically sharp interface with the monocrystalline oxide layer;

a second layer of electrically conductive non-magnetic material overlying the first layer and forming an atomically sharp interface with the first layer; and

a third layer of ferromagnetic material overlying the second layer and forming an atomically sharp interface with the second layer.

28. The structure of claim 27 wherein each of the first layer, second layer, and third layer comprises a layer of monocrystalline material.

29. The structure of claim 28 wherein each of the first layer, second layer, and third layer comprises a layer of epitaxially grown monocrystalline material.

30. The structure of claim 27 wherein the first layer comprises a material having a composition $(A_xB_{1-x})CO_3$ where A is selected from the group consisting of lanthanum and neodymium, B is selected from the group consisting of strontium, barium, calcium, and lead and x ranges from 0 to 1, and C is selected from the group consisting of Mn, (Mn_yCo_{1-y}) where y is greater than zero and less than or equal to 1, and (Mn_zNi_{1-z}) where z is greater than 0 and equal to or less than 1.

31. The structure of claim 30 wherein the second layer comprises a layer of electrically conductive oxide.

32. The structure of claim 31 wherein the third layer comprises a material having a composition $(A_xB_{1-x})CO_3$ where A is selected from the group consisting of lanthanum and neodymium, B is selected from the group consisting of strontium, barium, calcium, and lead and x ranges from 0 to 1, and C is selected from the group consisting of Mn, (Mn_yCo_{1-y}) where y is greater than zero and less than or equal to 1, and (Mn_zNi_{1-z}) where z is greater than 0 and equal to or less than 1.

33. An integrated spin valve circuit comprising:

a monocrystalline silicon substrate;

an integrated logic circuit formed at least partially in the silicon substrate;

a first monocrystalline oxide layer epitaxially grown overlying the silicon substrate;

an amorphous oxide formed underlying the first monocrystalline oxide layer;

a second monocrystalline layer of ferromagnetic oxide epitaxially formed overlying the monocrystalline oxide;

a third monocrystalline layer of electrically conductive non-magnetic oxide material overlying the second monocrystalline layer;

a fourth monocrystalline layer of ferromagnetic oxide epitaxially formed overlying the third monocrystalline layer; and

an electrical interconnect coupling the integrated logic circuit and the third monocrystalline layer.

34. The circuit of claim 33 wherein the integrated logic circuit comprises a CMOS circuit.

35. The circuit of claim 33 wherein the first monocrystalline oxide layer comprises a material selected from the group consisting of alkali earth metal titanates, zirconates, hafnates, tantalates, ruthenates, niobates and vanadates, perovskites including tin based perovskites, lanthanum aluminate, lanthanum scandium oxide, and gadolinium oxide.

36. The circuit of claim 35 wherein the first monocrystalline oxide layer comprises an alkali earth metal titanate.

37. The circuit of claim 35 wherein the first monocrystalline oxide layer comprises $Sr_gBa_{1-g}TiO_3$ where g ranges from 0 to 1.

38. The circuit of claim 35 wherein the second monocrystalline layer comprises $(A_xB_{1-x})CO_3$ where A is selected from the group consisting of lanthanum and neodymium, B is selected from the group consisting of strontium, barium, calcium, and lead and x ranges from 0 to 1, and C is selected from the group consisting of Mn, (Mn_yCo_{1-y}) where y is greater than zero and less than or equal to 1, and (Mn_zNi_{1-z}) where z is greater than 0 and equal to or less than 1.

39. The circuit of claim 38 wherein the fourth monocrystalline layer comprises $(A_xB_{1-x})CO_3$ where A is selected from the group consisting of lanthanum and neodymium, B is selected from the group consisting of strontium, barium, calcium, and lead and x ranges from 0 to 1, and C is selected from the group consisting of Mn, (Mn_yCo_{1-y}) where y is greater than zero and less than or equal to 1, and (Mn_zNi_{1-z}) where z is greater than 0 and equal to or less than 1.

40. The circuit of claim 35 wherein the third monocrystalline layer comprises a material selected from the group consisting of $(La_kSr_{1-k})CoO_3$ where k is greater than 0 and less than 1 and $SrVO_3$.

41. The circuit of claim 33 wherein the amorphous oxide comprises silicon oxide.

42. The circuit of claim 33 further comprising:

a fifth monocrystalline layer of electrically conductive non-magnetic oxide material overlying the fourth monocrystalline layer;

a sixth monocrystalline layer of ferromagnetic oxide epitaxially formed overlying the fifth monocrystalline layer; and

an electrical interconnect coupling the fifth monocrystalline layer and the third monocrystalline layer.

43. A process for fabricating an integrated spin valve circuit comprising the steps of:

providing a monocrystalline semiconductor substrate;

forming an integrated logic circuit at least partially in the semiconductor substrate;

forming a first template layer overlying the semiconductor substrate;

epitaxially growing a monocrystalline insulator layer overlying the first template layer;

forming an amorphous oxide layer underlying the monocrystalline insulator layer during the step of epitaxially growing the monocrystalline insulator layer;

forming a second template layer overlying the monocrystalline insulator layer;

epitaxially growing a first ferromagnetic oxide layer overlying the second template layer;

epitaxially growing an electrically conductive non-magnetic oxide layer overlying the first ferromagnetic oxide layer;

epitaxially growing a second ferromagnetic oxide layer overlying the electrically conductive non-magnetic oxide layer;

photolithographically patterning the first ferromagnetic oxide layer, the electrically conductive non-magnetic oxide layer and the second ferromagnetic

oxide layer to expose a portion of the integrated logic circuit; and

forming an electrical interconnect extending from the portion of the integrated logic circuit to the electrically conductive non-magnetic oxide layer.

44. The process of claim 43 wherein the step of providing a monocrystalline semiconductor substrate comprises the step of providing a substrate comprising silicon having a silicon oxide layer on a surface thereof and the step of forming a first template layer comprises the steps of:

depositing a material from the group consisting of alkali earth metals and alkali earth metal oxides onto the silicon oxide layer and

heating the substrate to react the material with the silicon oxide.

45. The process of claim 44 wherein the step of depositing a material from the group consisting of alkali earth metals and alkali earth metal oxides comprises depositing a material from the group consisting of barium, strontium, and mixtures of barium and strontium, and barium oxide, strontium oxide, and barium strontium oxide.

46. The process of claim 45 wherein the step of epitaxially growing a monocrystalline insulator layer comprises the steps of:

heating the monocrystalline semiconductor substrate to a temperature between about 200°C and about 800°C; and

introducing reactants comprising titanium, oxygen, and an element selected from strontium, barium, and strontium and barium.

47. The process of claim 46 wherein the step of introducing comprises controlling the ratio of strontium to titanium and controlling the partial pressure of oxygen.

48. The process of claim 47 wherein the step of forming an amorphous oxide layer comprises increasing the partial pressure of oxygen above a level necessary for epitaxially growing the monocrystalline insulator layer.

49. The process of claim 46 wherein the step of forming a second template layer comprises the step of capping the monocrystalline oxide layer with a layer comprising a monolayer of a material selected from the group consisting of titanium, titanium and oxygen, strontium, strontium and oxygen, barium, and barium and oxygen.

50. The process of claim 43 wherein the step of growing a monocrystalline insulator layer comprises the step of epitaxially growing by a process selected from the group consisting of MBE, MOCVD, MEE, CVD, PVD, PLD, CSD and ALE.

51. The process of claim 43 wherein the steps of epitaxially growing a first ferromagnetic oxide layer, epitaxially growing an electrically conductive non-magnetic oxide layer, and epitaxially growing a second ferromagnetic oxide layer each comprise the step of epitaxially growing by a process selected from the group consisting of MBE, MOCVD, MEE, CVD, PVD, PLD, CSD and ALE.

52. The process of claim 43 wherein the step of epitaxially growing a first ferromagnetic oxide layer comprises the step of growing an oxide layer of composition $(A_xB_{1-x})CO_3$ where A is selected from the group consisting of lanthanum and neodymium, B is selected from the group consisting of strontium, barium, calcium, and lead and x ranges from 0 to 1, and C is selected from the group consisting of Mn, (Mn_yCo_{1-y}) where y is greater than zero and less than or equal to 1, and (Mn_zNi_{1-z}) where z is greater than 0 and equal to or less than 1.

53. The process of claim 43 wherein the step of epitaxially growing a second ferromagnetic oxide layer comprises the step of growing an oxide layer of composition $(A_xB_{1-x})CO_3$ where A is selected from the group consisting of lanthanum and neodymium, B is selected from the group consisting of strontium, barium, calcium, and lead and x ranges from 0 to 1, and C is selected from the group consisting of Mn, (Mn_yCo_{1-y}) where y is greater than zero and less than or equal to 1, and (Mn_zNi_{1-z}) where z is greater than 0 and equal to or less than 1.

54. The process of claim 43 wherein the step of epitaxially growing an electrically conductive oxide layer comprises the step of growing an oxide layer having a composition selected from the group consisting of $(La_kSr_{1-k})CoO_3$ where k is greater than 0 and less than 1 and $SrVO_3$.

55. The process of claim 43 wherein the step of epitaxially growing a monocrystalline insulator layer comprises the step of growing a layer comprising a material selected from the group consisting of alkali earth metal titanates, zirconates, hafnates, tantalates, ruthenates, niobates and vanadates, tin based perovskites, lanthanum aluminate, lanthanum scandium oxide, gadolinium oxide, gallium nitride, and aluminum nitride.

56. The process of claim 55 wherein the step of epitaxially growing a first ferromagnetic oxide layer comprises the step of growing an oxide layer of composition $(A_xB_{1-x})CO_3$ where A is selected from the group consisting of lanthanum and neodymium, B is selected from the group consisting of strontium, barium, calcium, and lead and x ranges from 0 to 1, and C is selected from the group consisting of Mn, (Mn_yCo_{1-y}) where y is greater than zero and less than or equal to 1, and (Mn_zNi_{1-z}) where z is greater than 0 and equal to or less than 1.

57. The process of claim 56 wherein the step of forming a first template layer comprises the step of terminating the growth of the monocrystalline insulator layer with 1 - 10 monolayers of oxygen and a material selected from the group consisting of strontium, barium, calcium, and lead.

58. A process for fabricating a spin valve comprising the steps of:

providing a monocrystalline semiconductor substrate having a surface;

epitaxially growing a monocrystalline layer of insulator material on the surface;

epitaxially growing a first layer of ferromagnetic material overlying the monocrystalline layer of insulator material;

epitaxially growing a layer of non-magnetic conductive material overlying the first layer; and

forming a second layer of ferromagnetic material overlying the layer of non-magnetic conductive material.

59. The process of claim 58 wherein the step of epitaxially growing a first layer of ferromagnetic material comprises the step epitaxially growing a first layer of ferromagnetic material by a process selected from the group consisting of MBE, MOCVD, MEE, CVD, PVD, PLD, CSD and ALE.

60. The process of claim 59 wherein the step of epitaxially growing a first layer of ferromagnetic material comprises epitaxially growing a monocrystalline layer of ferromagnetic material.

61. The process of claim 58 wherein the step of forming a second layer comprises the step of forming a second layer by PVD.

62. The process of claim 61 wherein the step of forming a second layer comprises the step of forming a layer having an ordered crystalline structure.

63. A process for fabricating a spin valve circuit comprising the steps of:

providing a monocrystalline silicon substrate; and

depositing sequentially, by a process selected from the group consisting of MBE, MOCVD, MEE, CVD, PVD, PLD, CSD and ALE, the following monocrystalline epitaxial layers:

a layer of $Sr_gBa_{1-g}TiO_3$ where g ranges from 0 to 1;

a layer of ferromagnetic material of the composition $(A_xB_{1-x})CO_3$ where A is selected from the group consisting of lanthanum and neodymium, B is selected from the group consisting of strontium, barium, calcium, and lead and x ranges from 0 to 1, and C is selected from the group consisting of Mn, (Mn_yCo_{1-y}) where y is greater than zero and less than or equal to 1, and (Mn_zNi_{1-z}) where z is greater than 0 and equal to or less than 1;

a layer of electrically conductive non-magnetic oxide; and

a second layer of ferromagnetic material of the composition $(A_xB_{1-x})CO_3$ where A is selected from the group consisting of lanthanum and neodymium, B is selected from the group consisting of strontium, barium, calcium, and lead and x ranges from 0 to 1, and C is selected from the group consisting of Mn, (Mn_yCo_{1-y}) where y is greater than zero and less than or equal to 1, and (Mn_zNi_{1-z}) where z is greater than 0 and equal to or less than 1.

64. The process of claim 63 further comprising the step of forming a CMOS circuit at least partially in the silicon substrate.

65. The process of claim 64 further comprising the step of forming a strain relief layer underlying the layer of $Sr_gBa_{1-g}TiO_3$ where g ranges from 0 to 1.

66. The process of claim 64 further comprising the step of patterning the layer of ferromagnetic material, the layer of electrically conductive non-magnetic oxide, and the second layer of ferromagnetic material to form a magnetic sensor element.

67. The process of claim 66 further comprising the steps of:

depositing a layer of conductor material overlying the magnetic sensor element and the CMOS circuit; and

patterning the layer of conductor material to form an electrical interconnect configured to electrically couple the CMOS circuit and the magnetic sensor element.

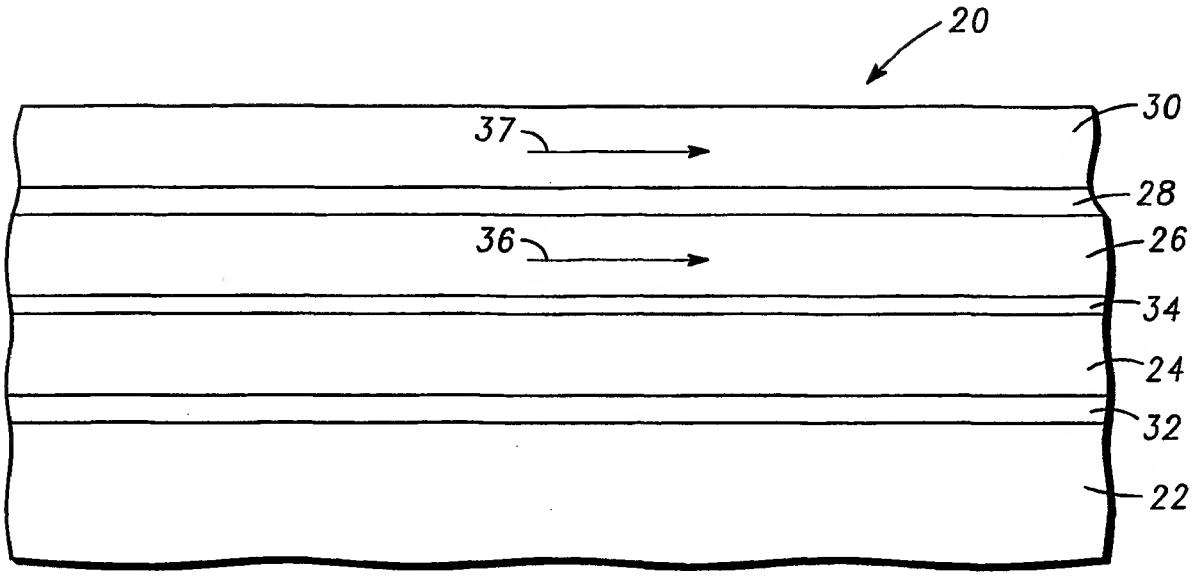


FIG. 1

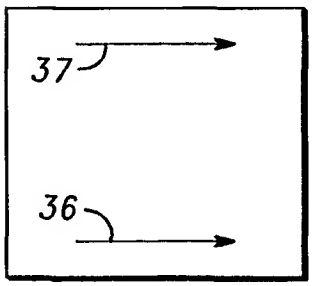


FIG. 2

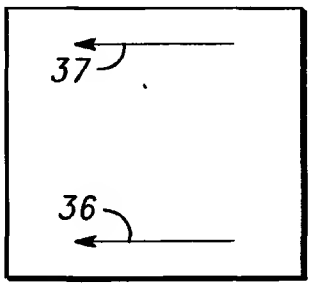


FIG. 3

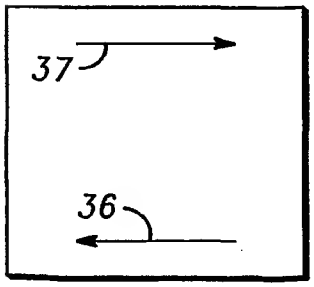


FIG. 4

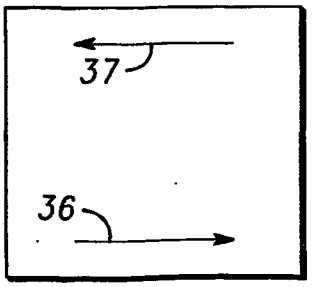


FIG. 5

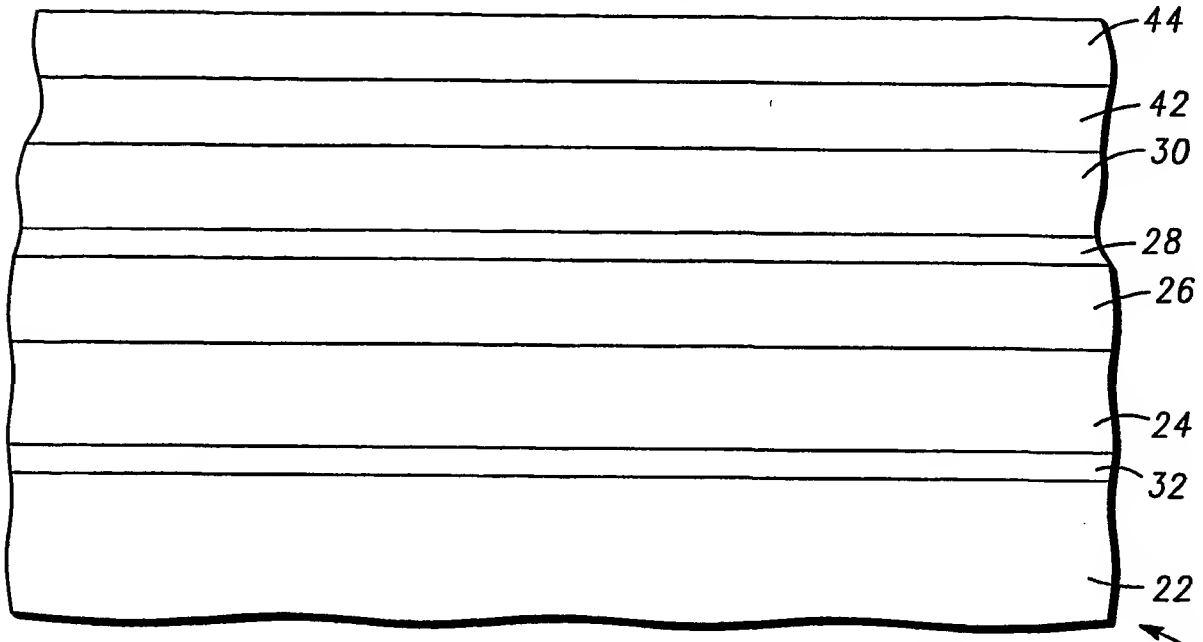


FIG. 6

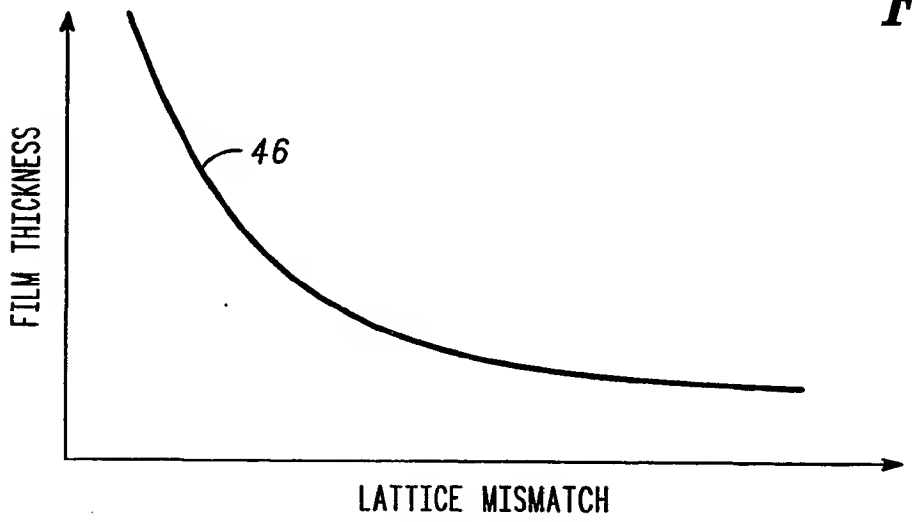
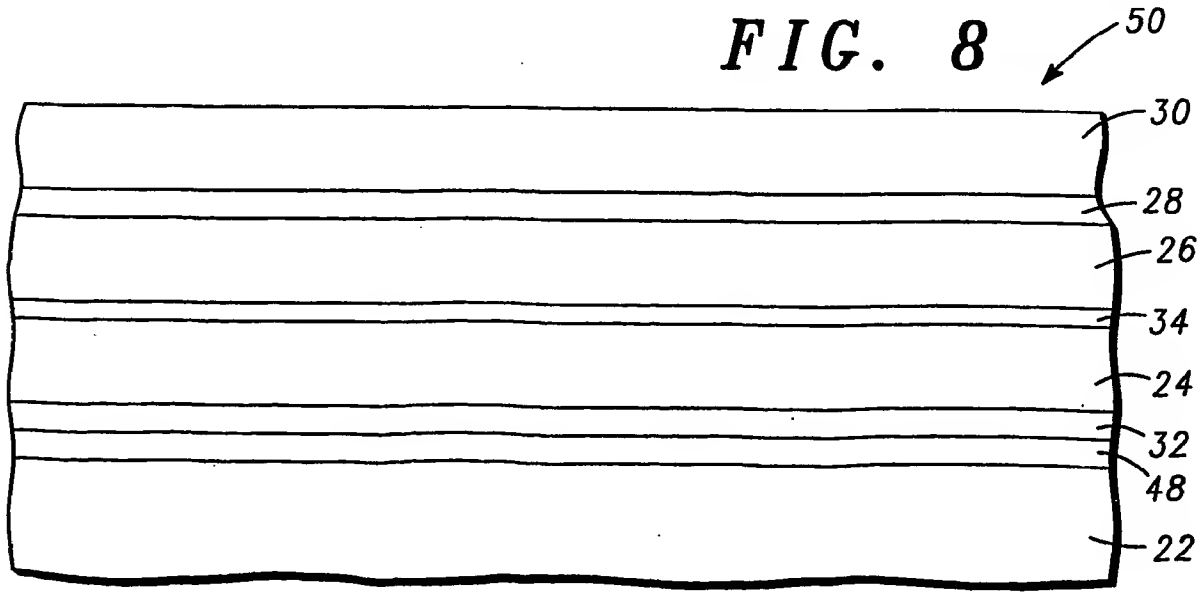


FIG. 7

FIG. 8



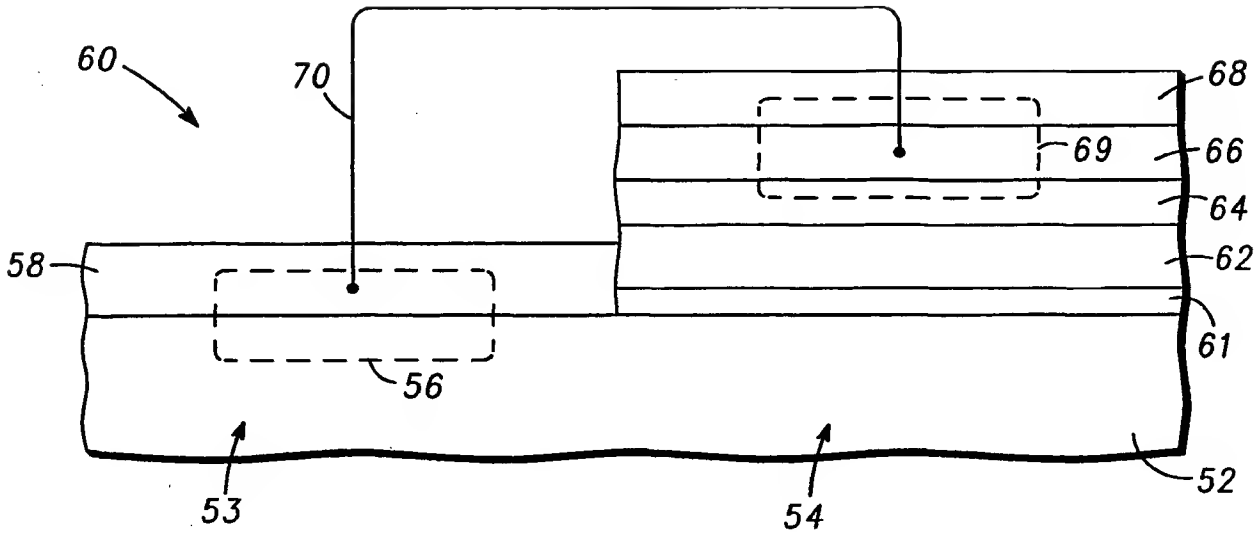


FIG. 9

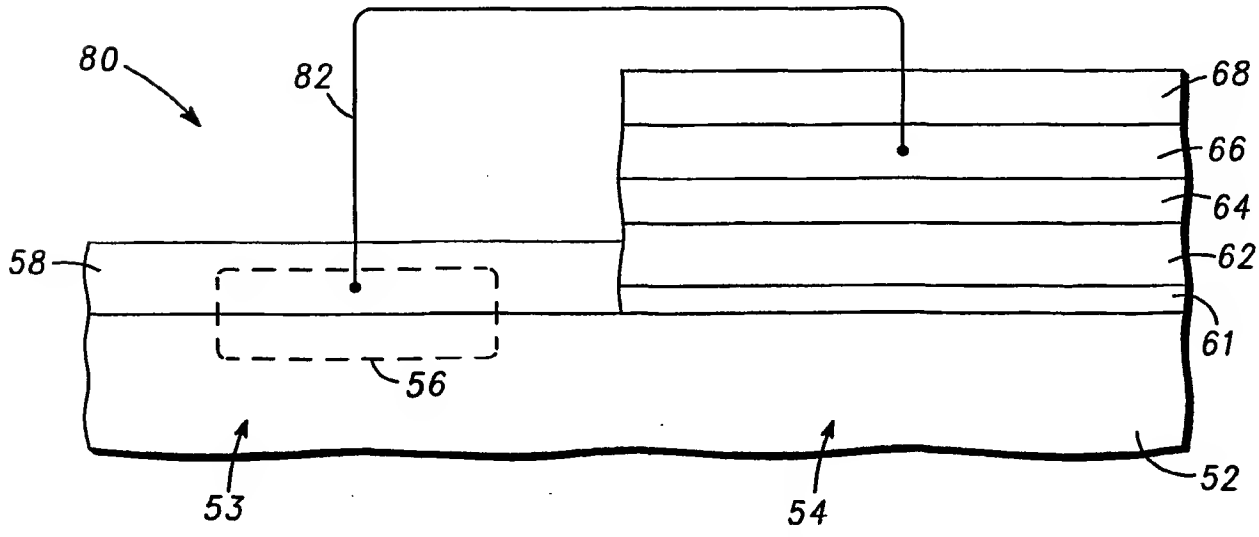


FIG. 10

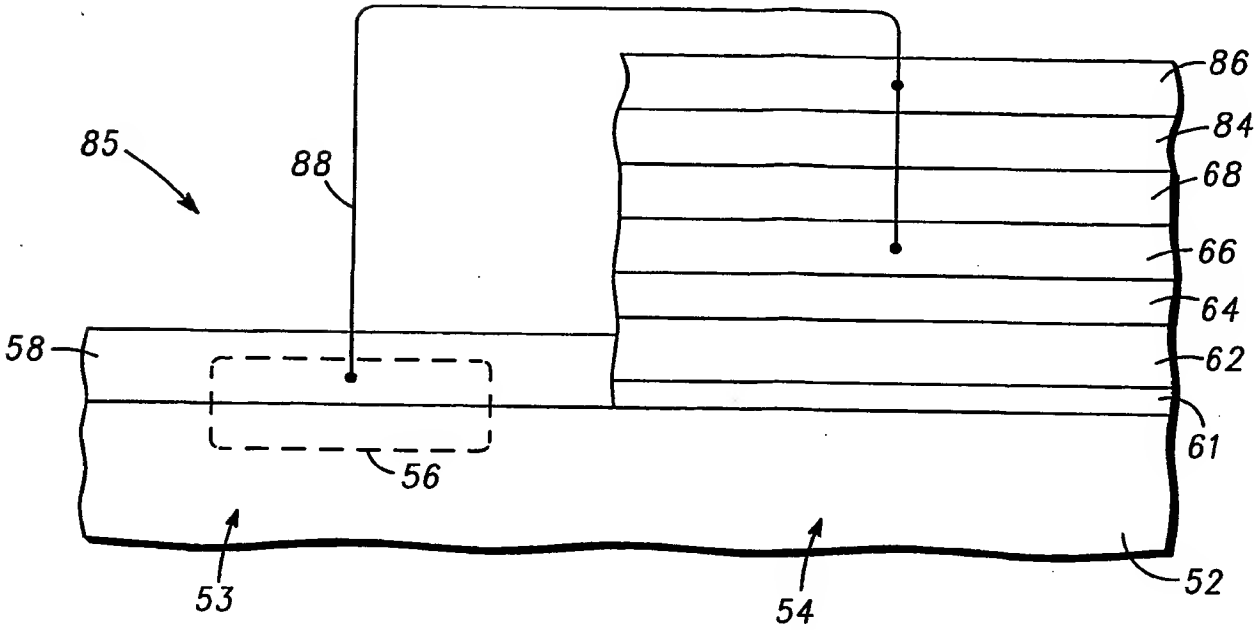


FIG. 11

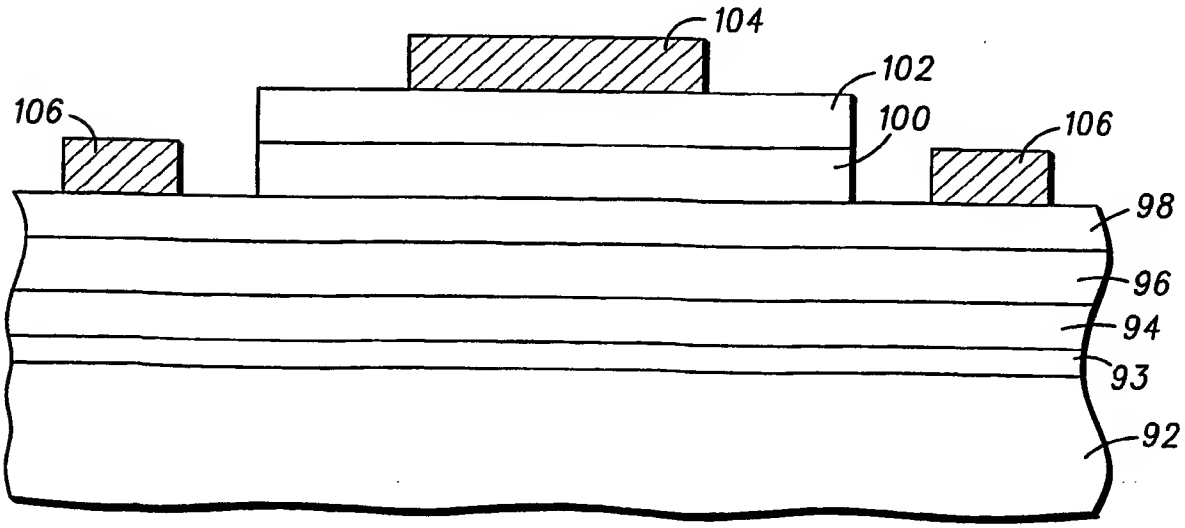


FIG. 12

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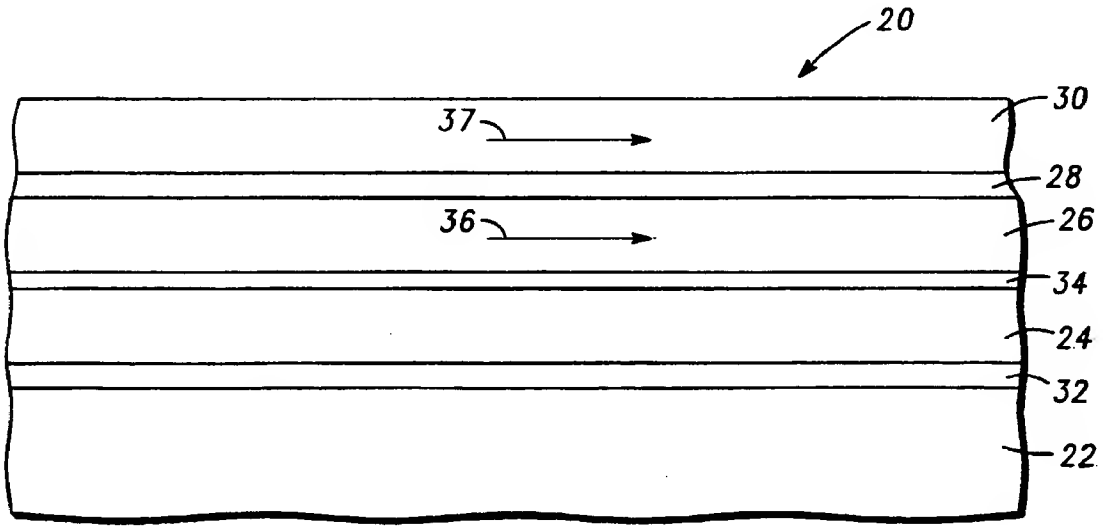
[Continued on next page]

(54) Title: SPIN VALVE STRUCTURE



(57) Abstract: A high GMR spin valve structure having multiple layers of a ferromagnetic material (26,30) and a conductive non-magnetic material (28) can be monolithically integrated with silicon circuits (50) by first growing an accommodating buffer layer (24) on a silicon wafer (22). The accommodating buffer layer is a layer of monocrystalline oxide spaced apart from the silicon wafer by an amorphous oxide layer (32) of silicon oxide. The amorphous oxide layer dissipates strain and permits the growth of a high quality monocrystalline oxide accommodating buffer layer. The accommodating buffer layer is lattice matched to both the underlying silicon wafer and the overlying ferromagnetic layer. Any lattice mismatch between the accommodating buffer layer and the underlying silicon substrate is taken care of by the amorphous oxide layer.

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

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Intern. nal Application No
PCT/US 01/22649

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01F10/32 H01L43/12 G11C11/16 H01F41/30 H01L43/08
H01L27/01

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01F H01L G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
PAJ, EPO-Internal, WPI Data, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	PATENT ABSTRACTS OF JAPAN vol. 2000, no. 03, 30 March 2000 (2000-03-30) & JP 11 340542 A (SANYO ELECTRIC CO LTD), 10 December 1999 (1999-12-10) abstract	1,8
A	ZHANG W ET AL: "STRESS EFFECT AND ENHANCED MAGNETORESISTANCE IN LA0.67CA0.33MNO3-DELTA FILMS" PHYSICAL REVIEW, B. CONDENSED MATTER, AMERICAN INSTITUTE OF PHYSICS. NEW YORK, US, vol. 58, no. 21, PART 1, 1 December 1998 (1998-12-01), pages 14143-14146, XP000822984 ISSN: 0163-1829 page 14143, column 2 -page 14146, column 2	1,4,6,8, 9

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
17 January 2002	29/01/2002

Name and mailing address of the ISA	Authorized officer
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Interna. .al Application No
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	LI X W ET AL: "EPITAXIAL LAO.67SR0.33MNO3 MAGNETIC TUNNEL JUNCTIONS" JOURNAL OF APPLIED PHYSICS, AMERICAN INSTITUTE OF PHYSICS. NEW YORK, US, vol. 81, no. 8, PART 2B, 15 April 1997 (1997-04-15), pages 5509-5511, XP000701274 ISSN: 0021-8979 page 5509; figure 1 ---	1,8,9, 27,30
A	DAUGHTON J M ET AL: "APPLICATIONS OF SPIN DEPENDENT TRANSPORT MATERIALS" JOURNAL OF PHYSICS D. APPLIED PHYSICS, IOP PUBLISHING, BRISTOL, GB, vol. 32, no. 22, 21 November 1999 (1999-11-21), pages R169-R177, XP000947410 ISSN: 0022-3727 page R171, column 2, paragraph 2 -page R172, column 1, paragraph 1 ------	1,5,22, 33

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Information on patent family members

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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